In the Claims:

Claims 1-3 (Canceled).

4. (Currently amended) ~~The magnetic memory of claim 1, wherein the~~ An integrated circuit memory device, comprising:

at least one array of magnetic memory cells; and

a control circuit **[[**is**]]** configured to organize the at least one array of magnetic memory cells into zero fault sections and usable fault sections, and store ~~the unchanged~~ data without ECC encoding in the zero fault sections and data ~~the~~ with ECC encoding ~~encoded data~~ in the usable fault sections.

5. (Currently amended) ~~The magnetic memory of claim 1, wherein the~~ An integrated circuit memory device, comprising:

at least one array of magnetic memory cells; and

a control circuit **[[**is**]]** configured to organize the at least one array of magnetic memory cells into sections comprising zero fault sections and further configured to sort received data to thereby identify ~~the unchanged data comprises~~ fault intolerant data to be stored in the zero fault sections.

Claims 6-8 (Canceled).

9. (Currently amended) ~~The magnetic memory of claim 1, wherein the~~ An integrated circuit memory device, comprising:

at least one array of magnetic memory cells; and

a control circuit **[[**is**]]** configured to organize the at least one array of magnetic memory cells into zero fault sections, usable fault sections and heavy fault sections that are remapped into the zero fault sections and the usable fault sections.

10. (Currently amended) ~~The magnetic memory of claim 1, wherein the~~ An integrated circuit memory device, comprising:

at least one array of magnetic memory cells; and

a control circuit **[[**is**]]** configured to organize the at least one array of magnetic memory cells into sections comprising zero fault sections**[[**,**]]** and provide pointers for a sequence of the zero fault sections.

11. (Currently amended) ~~The magnetic memory of claim 1, wherein the~~ An integrated circuit memory device, comprising:

at least one array of magnetic memory cells; and

a control circuit **[[**is**]]** configured to organize the at least one array of magnetic memory cells into sections comprising zero fault sections and provide non-destructive reads in the zero fault sections.

Claim 12 (Canceled).

13. (Currently amended) ~~The magnetic memory of claim 1, wherein the~~ An integrated circuit memory device, comprising:

at least one array of magnetic memory cells; and

a control circuit **[[**is**]]** configured to organize the at least one array of magnetic memory cells into zero fault sections and usable fault sections**[[**,**]]** and swap usable fault sections with zero fault sections based on number of accesses during a predetermined period.

Claims 14-22 (Canceled).

23. (Currently amended) ~~The magnetic memory of claim 16, wherein the~~ A magnetic memory, comprising:

an array of magnetic memory cells; and

a control circuit configured to divide the array of magnetic memory cells into zero fault sections and usable fault sections, receive data and sort the received data into the zero fault sections and usable fault sections based on predetermined criteria, said control circuit further **[[**is**]]** configured to provide destructive reads in the zero fault sections and the usable fault sections.

24. (Currently amended) ~~The magnetic memory of claim 16, wherein the~~ A magnetic memory, comprising:

an array of magnetic memory cells; and

a control circuit configured to divide the array of magnetic memory cells into zero fault sections and usable fault sections, receive data and sort the received data into the zero fault sections and usable fault sections based on predetermined criteria, said control circuit further **[[**is**]]** configured to provide non-destructive reads in the zero fault sections.

Claims 25-30 (Canceled).

31. (New) An integrated circuit device, comprising:

at least one array of non-volatile memory cells; and

a control circuit configured to test said at least one array of non-volatile memory cells to identify at least one zero fault section of non-volatile memory cells that is free of memory cell defects and at least another usable fault section of non-volatile memory cells that has memory cell defects, said control circuit further configured to selectively store first data without ECC encoding in the at least one zero fault section of non-volatile memory cells and store second data with ECC encoding in the at least another usable fault section of non-volatile memory cells.

32. (New) The integrated circuit device of Claim 31, wherein said control circuit is further configured to utilize multiple different ECC encoding schemes when storing second data in the at least another usable fault section of non-volatile memory cells.

33. (New) The integrated circuit device of Claim 32, wherein said control circuit selects among the different ECC encoding schemes based on fault probabilities associated with the non-volatile memory cells within the at least another usable fault section of non-volatile memory cells.